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U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Date	Name	Class	Subclass	Filing Date if Appropriate
FWB	A	5,117,377	5/1992	Finman	700/2	608
FWB	B	5,479,440	12/1995	Esfahani	375	346
	C					
	D					
	E					
	F					

FOREIGN PATENT DOCUMENTS

	Document No.	Date	Country	Class	Subclass	Translation
G						
H						

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

FWB	I	"di/dt Noise in CMOS Integrated Circuits", Analog Interated Circuits and Signal Processing, 14, 1997, pp. 113-129.
	J	"EMI-Noise Analysis under ASIC Design Environment", Proc. ISPD '99, 1999, pp. 16-21.
	K	"Interconnect and Circuit Modeling Techniques for Full-Chip Power Noise Analysis", IEEE TRANSACTIONS ON COMPONENTS, PACKAGING, AND MANUFACTURING TECHNOLOGY-PART B. VOL. 21, NO. 3, AUGUST 1998, pp. 209-215.
	L	"Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design", Proc. 34 th DAC, Jun. 1997, pp. 1-6.
	M	"A Macroscopic Substrate Noise Model for Full Chip Mixed-Signal Design Verification", 1997 Symposium on VLSI Circuits Digest of Technical Papers, pp. 37-38.
	N	"Design Methodologies for Noise in Digital Integrated Circuits", Proc. 35 th DAC, Jun. 1998, pp. 94-99.
	O	"Transition Density, A Stochastic Measure of Activity in Digital Circuits", Proc. 28 th DAC, 1991, pp. 644-649.

Examiner:

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